CLAIMS:

1. A programmable non-volatile semiconductor memory device comprising a matrix of rows and columns of memory cells each comprising

- a bridge of two bridge transistors coupled in parallel, said bridge transistors being controllable by a first and second select signal via a first and second select line,
- a silicided polysilicium fuse resistor connected with its one end to said bridge and with its other end to a program line for programming the memory cell, and
- a read transistor being controllable by a third select signal via a third select line and being connected with one end to said bridge and said one end of said fuse resistor and with its other end to a sense line for sensing the memory cell.

2. A semiconductor memory device as claimed in claim 1, wherein said bridge transistors and said read transistor are NMOS, PMOS or CMOS transistors.

3. A semiconductor memory device as claimed in claim 1, said bridge comprises two NMOS transistors and wherein said read transistor is a PMOS transistor.

4. A semiconductor memory device as claimed in claim 1, wherein the sources of said bridge transistors are connected to a ground voltage and wherein the drains of said bridge transistors are connected together, to the one end of said fuse resistor and to the source of said read transistor.

5. A semiconductor memory device as claimed in claim 1, further comprising a number of sense amplifiers connected to different sense lines, wherein all read transistors of all memory cells of the same row or column are connected to the same sense line to which a common sense amplifier is connected.

6. A semiconductor memory device as claimed in claim 1,

further comprising means for generating said select signals for control of said transistors which are adapted for setting said first select signal active high in for reading a memory cell and for setting said second select signal active high for writing to a memory cell.